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1	1933	(power adj2 control\$3) with (read or write)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:36
2	6990	sleep adj mode	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:36
3	1170	hibernat\$3	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:36
4	8053	(sleep adj mode) or hibernat\$3	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:36
5	15	((power adj2 control\$3) with (read or write)) same ((sleep adj mode) or hibernat\$3)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:36
6	11195050	@ad<20001227	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:37
7	13	((power adj2 control\$3) with (read or write)) same ((sleep adj mode) or hibernat\$3)) and @ad<20001227	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:42
8	7450	wake-up or wake adj up	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:43
9	173	(wake-up or wake adj up) with wireless	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:43
10	0	((power adj2 control\$3) with (read or write)) and ((wake-up or wake adj up) with wireless)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:43
11	1179	(wake-up or wake adj up) and (notebook or laptop or portable adj computer)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:44
12	101	(wake-up or wake adj up) same (notebook or laptop or portable adj computer)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:44
13	39	(wake-up or wake adj up) with (notebook or laptop or portable adj computer)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 15:44
14	22	@ad<20001227 and ((wake-up or wake adj up) with (notebook or laptop or portable adj computer))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 16:05
15	277508	synchronize or synchronized or synchronization	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 16:06
16	4	(@ad<20001227 and ((wake-up or wake adj up) with (notebook or laptop or portable adj computer))) and (synchronize or synchronized or synchronization)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 16:24
17	1509	711/154.cc1s.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 16:24

18	1267	713/300.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 16:24
19	301	713/310.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 16:25
20	494	713/324.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 16:25
21	1805	713/300.ccls. or 713/310.ccls. or 713/324.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 16:25
22	16	((power adj2 control\$3) with (read or write)) and ((sleep adj mode) or hibernat\$3) and (713/300.ccls. or 713/310.ccls. or 713/324.ccls.)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 16:25
23	12	@ad<20001227 and (((power adj2 control\$3) with (read or write)) and ((sleep adj mode) or hibernat\$3) and (713/300.ccls. or 713/310.ccls. or 713/324.ccls.))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/13 16:25

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*Matsuyama, K.; Asada, H.; Ikeda, S.; Taniguchi, K.;*  
Magnetics, IEEE Transactions on, Volume: 33, Issue: 5, Sept. 1997  
Pages:3283 - 3285

[\[Abstract\]](#) [\[PDF Full-Text \(248 KB\)\]](#) [IEEE JNL](#)**2 The highlights in the nano world**

*Chun-yen Chang;*  
Proceedings of the IEEE, Volume: 91, Issue: 11, Nov. 2003  
Pages:1756 - 1764

[\[Abstract\]](#) [\[PDF Full-Text \(945 KB\)\]](#) [\[Full-Text HTML\]](#) [IEEE JNL](#)**3 The quest for the SPIN transistor**

*Zorpette, G.;*  
Spectrum, IEEE, Volume: 38, Issue: 12, Dec. 2001  
Pages:30 - 35

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*Flaherty, N.;*  
IEE Review, Volume: 49, Issue: 11, Nov. 2003  
Pages:50 - 53

[\[Abstract\]](#) [\[PDF Full-Text \(355 KB\)\]](#) [IEE JNL](#)**5 HeRMES: high-performance reliable MRAM-enabled storage**

*Miller, E.L.; Brandt, S.A.; Long, D.D.E.;*  
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**6 An IC process compatible nonvolatile magnetic RAM**

*Tang, D.D.; Wang, P.K.; Speriosu, V.S.; Le, S.; Fontana, R.E.; Rishton, S.;*  
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**8 Thermal stability dependence on states for multi-state MRAM**

*Yuankai Zheng; Jinjun Qiu; Kebin Li; Zaibing Guo; Yihong Wu;*  
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**9 Low resistance spin-dependent tunneling junctions with naturally oxidized tunneling barrier**

*Sin, K.; Mao, M.; Chien, C.; Funada, S.; Miloslavsky, L.; Tong, H.-C.; Gupta, S.;*  
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Pages:2818 - 2820

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**10 Effects of pumping time on GMR and coercivity of RF-sputtered MRAM dual spin-valves**

*Seongtae Bae; Matsushita, N.; Zurn, S.; Sheppard, L.R.D.; Torok, E.J.; Judy, J.H.;*  
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Pages:2853 - 2856

[\[Abstract\]](#) [\[PDF Full-Text \(108 KB\)\]](#) [IEEE JNL](#)

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**11 Effects of initial layer surface roughness on GMR performance of Si/Cu/NiFe/Cu/Co/Cu/NiFe dual spin-valves for MRAM**

*Seongtae Bae; Matsushita, N.; Zurn, S.; Sheppard, L.; Torok, E.J.; Judy, J.H.;*  
Magnetics, IEEE Transactions on , Volume: 36 , Issue: 5 , Sept 2000  
Pages:2850 - 2852

[\[Abstract\]](#) [\[PDF Full-Text \(60 KB\)\]](#) [IEEE JNL](#)

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**12 A generalized HSPICE<sup>TM</sup> macro-model for pinned spin-dependent-tunneling devices**

*Das, B.; Black, W.C., Jr.;*  
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**13 Proposal and experimental demonstration of magnetic tunnel junction connected in parallel with tunnel diode**

*Uemura, T.; Honma, S.; Marukame, T.; Yamamoto, M.;*  
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Pages:1549 - 1551

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**14 Resistance ratio read (R<sup>3</sup>) architecture for a burst operated 1.5V MRAM macro**

*Inaba, T.; Tsuchida, K.; Sugabayashi, T.; Tahara, S.; Yoda, H.;*  
Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003 , 21-24 Sept. 2003  
Pages:399 - 402

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**15 Empty square as a hard-layer for MRAM**

*Geerpuram, D.; Mani, A.S.; Ayloo, K.; Domanowski, A.; Metlushko, V.;*  
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Magnetics Conference, 2003. INTERMAG 2003. IEEE International , 28 March-3 April 2003

Pages:ED - 07

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VLSI Circuits, 2003. Digest of Technical Papers. 2003 Symposium on , 12-14 June 2003

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Durlam, M.; Naji, P.; Omair, A.; DeHerrera, M.; Calder, J.; Slaughter, J.M.; Engel, B.; Rizzo, N.; Grynkewich, G.; Butcher, B.; Tracy, C.; Smith, K.; Kyler, K.; Ren, J.; Molla, J.; Feil, B.; Williams, R.; Tehrani, S.; VLSI Circuits Digest of Technical Papers, 2002. Symposium on , 13-15 June 2002 Pages:158 - 161

[\[Abstract\]](#) [\[PDF Full-Text \(396 KB\)\]](#) **IEEE CNF****2 A 1-Mbit MRAM based on 1T1MTJ bit cell integrated with copper interconnects**

Durlam, M.; Naji, P.J.; Omair, A.; DeHerrera, M.; Calder, J.; Slaughter, J.M.; Engel, B.N.; Rizzo, N.D.; Grynkewich, G.; Butcher, B.; Tracy, C.; Smith, K.; Kyler, K.W.; Ren, J.J.; Molla, J.A.; Feil, W.A.; Williams, R.G.; Tehrani, S.; Solid-State Circuits, IEEE Journal of , Volume: 38 , Issue: 5 , May 2003 Pages:769 - 773

[\[Abstract\]](#) [\[PDF Full-Text \(1084 KB\)\]](#) **IEEE JNL****3 A 10 ns read and write non-volatile memory array using a magnetic tunnel junction and FET switch in each cell**

Scheuerlein, R.; Gallagher, W.; Parkin, S.; Lee, A.; Ray, S.; Robertazzi, R.; Reohr, W.; Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000 IEEE International , 7-9 Feb. 2000 Pages:128 - 129

[\[Abstract\]](#) [\[PDF Full-Text \(215 KB\)\]](#) **IEEE CNF****4 High speed (10-20 ns) non-volatile MRAM with folded storage elements**

Ranmuthu, K.T.M.; Ranmuthu, I.W.; Pohm, A.V.; Comstock, C.S.; Hassoun, M.; Magnetics, IEEE Transactions on , Volume: 28 , Issue: 5 , Sep 1992

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*Durlam, M.; Addie, D.; Akerman, J.; Butcher, B.; Brown, P.; Chan, J.; DeHerrera, M.; Engel, B.N.; Feil, B.; Grynkevich, G.; Janesky, J.; Johnson, M.; Kyler, K.; Molla, J.; Martin, J.; Nagel, K.; Ren, J.; Rizzo, N.D.; Rodriguez, T.; Savtchenko, L.; Salter, J.; Slaughter, J.M.; Smith, K.; Sun, J.J.; Lien, M.; Papworth, K.; Shah, P.; Qin, W.; Williams, R.; Wise, L.; Tehrani, S.;*

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**6 Fully integrated 64 Kb MRAM with novel reference cell scheme**

*Jeong, H.S.; Jeong, G.T.; Koh, G.H.; Song, I.H.; Park, W.J.; Kim, T.W.; Jeong, S.J.; Hwang, Y.N.; Ahn, S.J.; Kim, H.J.; Hong, J.S.; Jeong, W.C.; Lee, S.H.; Park, J.H.; Cho, W.Y.; Kim, J.S.; Song, S.H.; Park, S.O.; Jeong, U.I.; Kim, K.;*

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*Motoyoshi, M.; Moriyama, K.; Mori, H.; Fukumoto, C.; Itoh, H.; Kano, H.; Bessho, K.; Narisawa, H.;*

*VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on , 11-13 June 2002*

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**8 Optimizing Write Current and Power Dissipation in MRAMs by Using an Astroid Curve**

*Miyatake H. ; Sunaga T. ; Umezaki H. ; Asano H. ;*

*Transactions on Magnetics : Accepted for future publication , Volume: PP , Issue: 99 , 2004*

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*Au, E.K.S.; Ki, W.-H.; Mow, W.H.; Hung, S.T.; Wong, C.Y.;*

*Magnetics, IEEE Transactions on , Volume: 40 , Issue: 2 , March 2004*

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**10 Magnetostatic coupling in spin dependent tunnel junctions**

*Dexin Wang; Daughton, J.M.; Reed, D.; Wang, W.D.; Jian-Qing Wang;*

*Magnetics, IEEE Transactions on , Volume: 36 , Issue: 5 , Sept 2000*

Pages:2802 - 2805

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**11 A novel low power VMRAM/MTJ design with robust magnetic switching**

Xiaochun Zhu; Jian-Gang Zhu;

Magnetics Conference, 2003. INTERMAG 2003. IEEE International , 28 March-3 April 2003

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US-PAT-NO: 5954820

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TITLE: Portable computer with adaptive demand-driven power management

----- KWIC -----

Application Filing Date - AD (1):  
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Detailed Description Text - DETX (13):

The two common power-save modes are referred to as IDLE2 and STANDBY. In the IDLE2 mode, the actuator 63 is parked (i.e., moved to the outer edge of disk 60), and the servo control electronics 53 and read electronics, including preamplifier and channel 54, are turned off. The IDLE2 mode thus substantially reduces or removes power to servo control electronics 53, preamplifier and channel 54. In the IDLE2 power-save mode, it is also possible to reduce power to controller 56 because the servo and read tasks are not active. In the STANDBY mode, the actuator 63 is moved to its parking location and the spindle motor 62 and spindle driver 51 are turned off. The STANDBY power-save mode has all the power savings of IDLE2, plus the additional reduction in power to spindle control electronics portion of controller 56 and spindle driver 51. In some implementations, buffer 57 may also be turned off in one or both of the IDLE2 and STANDBY modes. Additional power-save modes are also possible. For example, the SLEEP mode includes the power-save features of STANDBY and also has almost all remaining electronics turned off, leaving powered on only a portion of the controller 56 and whatever else is necessary to respond to a SLEEP recovery command from computer IDE controller 6 (FIG. 1).